SPECIFICATIONS

CIO-DAS16/330

Analog Input & Digital I/O

Revision 4, October, 2001

Power Consumption

+5V:	900 mA typical, mA max

Analog Input Section

A/D converter type	AD7800
Resolution	12 bits
Number of channels	8 differential or 16 single-ended, switch-selectable
Programmable ranges	±10V, ±5V, ±2.5V, ±1.25V , ±0.625V, 0 to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.25V, 0 to 0.625V, fully programmable
Polarity	Unipolar/Bipolar, software-selectable
A/D pacing	Programmable: internal counter or external source (DIG. IN 0 / TRIGGER, rising edge) or software-polled
A/D Trigger sources	External hardware/software (DIG. IN 0 / TRIGGER, active high)
A/D Triggering Modes	
Digital:	Gated pacer, software-polled. (Gate must be disabled by software after trigger event.)
Data transfer	From 512 sample FIFO via REPINSW, interrupt, DMA or software polled
DMA	Channel 1 or 3, switch-selectable
A/D conversion time	3 µs
Throughput	330 kHz
Absolute accuracy	0.01% of reading ±1 LSB
Differential Linearity error	±1 LSB
Integral Linearity error	±1 LSB
Differential Linearity error	±1 LSB
No missing codes guaranteed	12 bits
Gain drift (A/D specs)	±25 ppm/°C
Zero drift (A/D specs)	±10 ppm/°C
Common Mode Range	±10V
CMRR @ 60 Hz	–72dB
Input leakage current	200 nA (@25 Deg C)
Input impedance	10 MegOhms min
Absolute max. input voltage	±35V

Digital Input / Output

Digital type:	
Input:	74LS367
Output:	74LS197
Configuration	Two ports, 4 input bits and 4 output bits
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.5V max (IOL = 8 mA)
Output high voltage	2.7V min (IOH = –0.4 mA)
Absolute max. input voltage	–0.5V, +7V

Interrupts	2 through 7, 10 and 11, programmable
Interrupt enable	Programmable
Interrupt sources	A/D End-of-conversion, A/D FIFO-half-full, Residual counter, DMA terminal count

Counter Section

Counter type	82C54
Configuration	Two 82C54 devices, 3 down-counters each device; 16 bits each.

82C54A:

Counter 0 - Independent, available to user
- Source: 100 kHz on board clock or external (CTR 0 Clock In)
- Gate: External (Dig In 2 / CTR 0 Gate)
- Output: Available at user connector (CTR 0 Out)

Counter 1 - ADC Pacer Lower Divider
- Source: 1 or 10 MHz oscillator, jumper-selectable
- Gate: Tied to Counter 2 gate, programmable source (internal or external (Dig In 0 / Trigger).
- Output: Chained to Counter 2 Clock.

Counter 2 - ADC Pacer Upper Divider
- Source: Counter 1 Output.
- Gate: Tied to Counter 1 gate, programmable source: internal or external (Dig In 0 / Trigger).
- Output: ADC Pacer clock, available at user connector (CTR 2 Out)

82C54B:

Counter 0 - Total samples (residual) counter upper divider
- Source: Counter 1 output (total samples lower divider)
- Gate: Internal
- Output: Internal

Counter 1 - Total samples (residual) counter lower divider
- Source: ADC conversion complete
- Gate: Tied to Counter 2 gate, internal source.
- Output: Counter 0 input (total samples upper divider)

Counter 2 - Trigger index counter
- Source: ADC conversion complete
- Gate: Tied to Counter 1 gate, internal source.
- Output: Not used

Clock input frequency	10 MHz max
High pulse width (clock input)	30 ns min
Low pulse width (clock input)	50 ns min
Gate width high	50 ns min
Gate width low	50 ns min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min
Crystal Oscillator Frequency	10 MHz
Frequency accuracy	100 ppm

Environmental

Operating temperature range	0 to 50°C
Storage temperature range	–20 to 70°C
Humidity	0 to 90% non-condensing

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