PCI-DAS6052

Analog Input and Digital I/O

Specifications

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MEASUREMENT COMPUTING™

PCI-DAS6052 Specifications

All specifications are subject to change without notice.
Typical for 25 °C unless otherwise specified.
Specifications in *italic text* are guaranteed by design.

Analog input

Table 1. Analog input specifications

Parameter	Specification
A/D converter	Successive approximation type, 333 kS/s conversion rate.
Resolution	16 bits, 1 in 65536
Maximum sample rate	333 kS/s
Number of channels	16 single ended / 8 differential, software selectable
Input ranges	Bipolar: ±10V, ±5V, ±2.5V, ±1V, ±0.5V, ±0.25V, ±0.1V, ±0.05V, Unipolar: 0 to 10V, 0 to 5V, 0 to 2V, 0 to 1V, 0 to 0.5V, 0 to 0.2V, 0 to 0.1V Software selectable
A/D pacing	Internal counter – ASIC. Software selectable time base: ▪ Internal 40 MHz, 50 ppm stability ▪ External source via AUXIN<5:0>, software selectable.
	External convert strobe: A/D CONVERT
	Software paced
Burst mode	Software selectable option, burst rate = 3 µS
A/D gate sources	External digital: A/D GATE
	External analog: ATRIG input CH0 IN through CH15 IN
A/D gating modes	External digital: Programmable, active high or active low, level or edge
	External analog: Refer to the *Analog trigger* section on page 8
A/D trigger sources	External digital: A/D START TRIGGER A/D STOP TRIGGER
	External analog: ATRIG input CH0 IN through CH15 IN
A/D triggering modes	External digital: Software-configurable for rising or falling edge.
	External analog: Refer to the *Analog trigger* section on page 8
	Pre-/post-trigger: Unlimited number of pre-trigger samples, 16 Meg post-trigger samples.
ADC pacer out	Available at user connector: A/D PACER OUT
RAM buffer size	8 K samples
Data transfer	DMA
	Programmed I/O
DMA modes	Demand or non-demand using scatter-gather
Configuration memory	Up to 8 K elements. Programmable channel, gain, and offset
Streaming-to-disk rate	333 kS/s, system dependent

Accuracy

333 kS/s sampling rate, single channel operation and a 15-minute warm-up. Accuracies listed are for measurements made following an internal calibration. They are valid for operational temperatures within ±1 °C of internal calibration temperature and ±10 °C of factory calibration temperature. Calibrator test source high side tied to Channel 0 high and low side tied to Channel 0 how. Low-level ground is tied to Channel 0 low at the user connector.

Table 2. Absolute accuracy specifications

Range	Absolute Accuracy
±10 V	±15.6 LSB
±5 V	±5.7 LSB
±2.5 V	±15.6 LSB
±1 V	±15.7 LSB
±500 mV	±15.9 LSB
±250 mV	±18.0 LSB
±100 mV	±21.0 LSB
±50 mV	±23.0 LSB
0 to 10 V	±8.1 LSB
0 to 5 V	±27.8 LSB
0 to 2 V	±28.0 LSB
0 to 1 V	±28.0 LSB
0 to 500 mV	±31.7 LSB
0 to 200 mV	±36.4 LSB
0 to 100 mV	±38.7 LSB

Table 3. Absolute accuracy components – all values are (±)

Range	% of Reading	Offset (µV)	Noise +Quantization (µV)		Temp Drift (%/DegC)	Absolute Accuracy at FS (mV)
			Single Pt	Averaged (Note 1)		
±10V	0.0371	947	981	87.0	0.0006	4.747
±5V	0.0071	476	491	43.5	0.0001	0.876
±2.5V	0.0371	241	245	21.7	0.0006	1.190
±1V	0.0371	99.2	98.1	8.7	0.0006	0.479
±500mV	0.0371	52.1	56.2	5.0	0.0006	0.243
±250mV	0.0421	28.6	32.8	3.0	0.0006	0.137
±100mV	0.0471	14.4	22.4	2.1	0.0006	0.064
±50mV	0.0471	9.7	19.9	1.9	0.0006	0.035
0 to 10V	0.0071	476	491	43.5	0.0001	1.232
0 to 5V	0.0371	241	245	21.7	0.0006	2.119
0 to 2V	0.0371	99.2	98.1	8.7	0.0006	0.850
0 to 1V	0.0371	52.1	56.2	5.0	0.0006	0.428
0 to 500mV	0.0421	28.6	39.8	3.0	0.0006	0.242
0 to 200mV	0.0471	14.4	22.4	2.1	0.0006	0.111
0 to 100mV	0.0471	9.7	19.9	1.9	0.0006	0.059

Note 1: Averaged measurements assume averaging of 100 single-channel readings

Each PCI-DAS6052 is tested at the factory to assure the board's overall error does not exceed accuracy limits described in Table 2.

Table 4. Relative accuracy specifications – all values are (±)

Range	Relative Accuracy (µV)	
	Single Point	**Averaged (Note 2)**
±10 V	1145	115
±5 V	573	57.3
±2.5 V	286	28.6
±1 V	115	11.5
±500 mV	66.3	6.6
±250 mV	39.2	3.9
±100 mV	27.7	2.8
±50 mV	25.3	2.5
0 to 10 V	573	57.3
0 to 5 V	286	28.6
0 to 2 V	115	11.5
0 to 1 V	66.3	6.6
0 to 500 mV	48.2	3.9
0 to 200 mV	27.7	2.8
0 to 100 mV	25.3	2.5

Note 2: Averaged measurements assume averaging of 100 single-channel readings

Relative accuracy is defined as the measured deviation from a straight line drawn between measured endpoints of the transfer function. ADC resolution, noise and front-end non-linearity are included in this measurement.

Table 5. Differential non-linearity specifications

All Ranges	±0.5 LSB typ	±1.0 LSB max

Settling time

Settling time is defined as the time required for a channel to settle to within a specified accuracy in response to a full-scale (FS) step. Two channels are scanned at the specified rate. A –FS DC signal is presented to Channel 1; a +FS DC signal is presented to Channel 0.

Table 6. Settling time specifications

Condition	Range	Accuracy				
		±0.00076% (±0.5 LSB)	**±0.0015% (±1 LSB)**	**±0.0031% (±2 LSB)**	**±0.0061% (±4 LSB)**	**±0.024% (±16 LSB)**
Same range to same range	±10 V	20 µS typ	10 µS max	5 µS max	4 µS max	3 µS typ
	±5 V	20 µS typ	10 µS max	5 µS max	4 µS max	3 µS typ
	±2.5 V	20 µS typ	10 µS max	5 µS max	4 µS max	3 µS typ
	±1 V	20 µS typ	10 µS max	5 µS max	4 µS max	3 µS typ
	±500 mV	20 µS typ	10 µS max	5 µS max	4 µS max	3 µS typ
	±250 mV	20 µS typ	10 µS max	5 µS max	4 µS max	3 µS typ
	±100 mV	20 µS typ	10 µS max	5 µS max	4 µS max	3 µS typ
	±50 mV	20 µS typ	10 µS max	5 µS max	4 µS max	3 µS typ
	0 to 10 V	20 µS typ	10 µS max	5 µS max	4 µS max	3 µS typ
	0 to 5 V	20 µS typ	10 µS max	5 µS max	4 µS max	3 µS typ
	0 to 2 V	20 µS typ	10 µS max	5 µS max	4 µS max	3 µS typ
	0 to 1 V	20 µS typ	15 µS max	5 µS max	4 µS max	3 µS typ
	0 to 500 mV	20 µS typ	15 µS max	8 µS max	4 µS max	3 µS typ
	0 to 200 mV	20 µS typ	15 µS max	8 µS max	4 µS max	3 µS typ
	0 to 100 mV	20 µS typ	15 µS max	10 µS max	4 µS max	3 µS typ

Parametrics

Table 7. Parametric specifications

Max working voltage (signal + common-mode)	±11 V	
CMRR @ 60 Hz	±10 V range:	92 dB
	0 to 10 V and ±5 V range:	97 dB
	0 to 5 V and ±2.5 V range:	101 dB
	0 to 2 V and ±1 V range:	104 dB
	0 to 1 V and ±0.5 V range:	105 dB
	0 to 0.5 V and ±0.25 V range:	105 dB
	0 to 0.5 V and ±0.1 V range:	105 dB
	0 to 0.1 V and ±0.05 V range:	105 dB
Small signal bandwidth, all ranges	*480 kHz*	
Input coupling	*DC*	
Input impedance	*100 GΩ in parallel with 100 pF in normal operation.*	
Input bias current	*±200 pA*	
Input offset current	*±100 pA*	
Absolute maximum input voltage	*Power ON: ±25 V, Power OFF: ±15 V (±20 mA; Note 3)* *Protected inputs:* ▪ *CH<15:0> IN* ▪ *AISENSE*	
Power on and reset state	CH0 IN, single-ended mode, 0 V to 0.1 V input range (Note 4)	
Crosstalk	Adjacent channels: –75 dB	
	All other channels: –90 dB	

Note 3: The analog input sink/source current must be limited to an maximum of ±20 mA in the power OFF state to prevent damage to the board. A 1000 Ω (¼ W) current limiting resistor should be placed in series with each analog input channel being used in applications where the power OFF state sink/source current into the board can exceed ±20 mA. Resistance values >1000 Ω may adversely affect the noise and settling time performance of the board.

Note 4: Care should be taken to avoid the application of an input voltage to CH0 IN that could overdrive the analog input circuit. Any unused analog input channel should be connected to LLGND.

Noise performance

Table 8 summarizes the noise performance for the PCI-DAS6052. Noise distribution is determined by gathering 50 K samples with inputs tied to ground at the user connector. Samples are gathered at the maximum specified single channel sampling rate. Specification applies to differential mode operation.

Table 8. Analog input noise performance specifications

Range	LSBrms	Typical Counts
±10 V	0.95	11
±5 V	0.95	11
±2.5 V	0.95	11
±1 V	0.95	11
±500 mV	1.1	11
±250 mV	1.3	13
±100 mV	2.3	23
±50 mV	4.2	42
0 to 10 V	0.95	11
0 to 5 V	0.95	11
0 to 2 V	0.95	11
0 to 1 V	1.1	11

Range	LSBrms	Typical Counts
0 to 500 mV	1.3	13
0 to 200 mV	2.3	23
0 to 100 mV	4.2	42

Analog output

Table 9. Analog output specifications

Parameter	Specification
D/A converter type	Double-buffered, multiplying
Resolution	16-bits, 1 in 65536
Number of channels	2, voltage output type
Voltage range	±10 V, 0 to 10 V, ±EXT REF., 0 to EXT REF., software selectable
Monotonicity	*16-bits, guaranteed*
Slew rate	15 V/µs typ.
Settling time (full scale step)	3.5 µs max to ±1 LSB
Noise	60 µVrms, DC to 1 MHz BW
Glitch energy	*±10 mV with 1 µS duration (measured at mid-scale transition)*
Current drive	±5 mA
Output short-circuit duration	*Indefinite @ 25 mA*
Output coupling	*DC*
Output impedance	0.1 Ω max
Power up and reset	DACs cleared to 0 volts ±20 mV max.

Table 10. Absolute accuracy specifications

Range	Absolute Accuracy
±10 V	±4.6 LSB
0 to 10 V	±7.7 LSB

Table 11. Absolute accuracy components specifications - all values are (±)

Range	% of Reading	Offset (µV)	Temp Drift (%/DegC)	Absolute Accuracy at FS (mV)
±10 V	0.0061	798	0.0001	1.405
0 to 10 V	0.0061	569	0.0001	1.176

Each PCI-DAS6052 is tested at the factory to ensure that the overall error does not exceed the values specified in Table 10.

Table 12. Relative accuracy specifications

Range	Relative Accuracy	
All ranges	±0.35 LSB, typ	±1.0 LSB, max

Relative accuracy is defined as the measured deviation from a straight line drawn between measured endpoints of the transfer function.

Analog output pacing and triggering

Table 13. AO pacing and triggering specifications

Parameter	Specification
DAC pacing (SW programmable)	Internal counter – ASIC. Selectable time base: ▪ Internal 40 MHz, 50 ppm stability. ▪ External Source via AUXIN<5:0>, SW selectable.
	External convert strobe: D/A UPDATE
	Software paced
DAC gate sources (Software programmable)	External digital: D/A START TRIGGER
	External analog: ATRIG input CH0 IN through CH15 IN
	Software gated
DAC gating modes	External digital: Programmable, active high or active low, level or edge
	External analog: Refer to the Analog trigger section on page 8
DAC trigger sources	External digital: D/A START TRIGGER
	External analog: ATRIG input CH0 IN through CH15 IN
	Software triggered
DAC triggering modes	External digital: Software-configurable for rising or falling edge
	External analog: Refer to the Analog trigger section on page 8
DAC pacer out	Available at user connector D/A PACER OUT
RAM buffer size	16 K samples
Data transfer	DMA
	Programmed I/O
	Update DACs individually or simultaneously, software selectable
DMA modes	Demand or Non-demand using scatter gather
Waveform generation throughput	333 kS/s max per channel, 2 channels simultaneous

Analog output external reference input (D/A EXTREF)

Table 14. External reference input (D/A EXTREF) specifications

Parameter	Specification
Range	±11 V
Overvoltage protection	±25 V powered on, ±15 V powered off
Input Impedance	10 kΩ min
Bandwidth (-3 dB)	3 kHz
Slew rate	0.3 V/µS

Analog trigger

Table 15. Analog trigger specifications

Parameter	Specification	
Analog trigger sources Software selectable	External: ATRIG input CH0 IN through CH15 IN, first channel in scan	
Analog trigger levels	ATRIG input: ±10V	
	CH0 IN through CH15 IN: ± Full-scale, range dependent	
Analog trigger modes	External analog: software-configurable for: ▪ Positive or negative slope	
Analog gate modes	External analog: Software-configurable for: ▪ Above or below reference ▪ Positive or negative hysteresis ▪ In or out of window	
Resolution	12-bits, 1-in-4096	
Accuracy	±1% full-scale range max	
Bandwidth (-3dB)	ATRIG input	700 kHz
	CH0 IN through CH15 IN	700 kHz

Analog I/O calibration

Table 16. Analog I/O calibration specifications

Parameter	Specification
Recommended warm-up time	15 minutes
Calibration	Auto-calibration, calibration factors for each range stored on board in non-volatile RAM.
Onboard calibration reference	*DC Level: 5.000 V± 1 mV. Actual measured values stored in EEPROM.*
	Tempco: 0.6 ppm/°C max
	Long-term stability: ±6 ppm/sqrt (1000 hrs)
Calibration interval	1 year

Digital I/O

Table 17. DIO specifications

Parameter	Specification
Digital type	Discrete, 5V/TTL compatible
Number of I/O	8
Configuration	8 bits, independently programmable for input or output. All pins pulled up to +5 V via 47 K resistors (default). Positions available for pull-down to ground. Hardware selectable via solder gap.
Input high voltage	2.0 V min, 7.0 V absolute max
Input low voltage	0.8 V max, –0.5 V absolute min
Output high voltage (IOH = -32 mA)	3.80 V min, 4.20 V typ
Output low voltage (IOL = 32 mA)	0.55 V max, 0.22 V typ
Data transfer	Programmed I/O
Power-up / reset state	Input mode (high impedance)

Interrupts

Table 18. Interrupt specifications

Parameter	Specification
Interrupts	PCI INTA# - mapped to IRQn via PCI BIOS at boot-time
Interrupt enable	Programmable through PLX9080
ADC Interrupt sources (software programmable)	DAQ_ACTIVE: Interrupt is generated when a DAQ sequence is active.
	DAQ_STOP: Interrupt is generated when A/D Stop Trigger In is detected.
	DAQ_DONE: Interrupt is generated when a DAQ sequence completes.
	DAQ_FIFO_1/4_FULL: Interrupt is generated when ADC FIFO is ¼ full.
	DAQ_SINGLE: Interrupt is generated after each conversion completes.
	DAQ_EOSCAN: Interrupt is generated after the last channel is converted in multi-channel scans.
	DAQ_EOSEQ: Interrupt is generated after each interval delay during multi-channel scans.
DAC Interrupt sources (software programmable)	DAC_ACTIVE: Interrupt is generated when DAC waveform circuitry is active.
	DAC_DONE: Interrupt is generated when a DAC sequence completes.
	DAC_FIFO_1/4_EMPTY: Interrupt is generated DAC FIFO is ¼ empty.
	DAC_HIGH_CHANNEL: Interrupt is generated when the DAC high channel output is updated.

Counters

Table 19. Counter specifications

Parameter	Specification
User counter type	82C54
Number of channels	2
Resolution	16-bits
Compatibility	5V/TTL
CTRn base clock source (software selectable)	Internal 10 MHz, Internal 100 kHz or external connector (CTRn CLK)
Internal 10 MHz clock source stability	50 ppm
Counter n gate	Available at connector (CTRn GATE).
Counter n output	Available at connector (CTRn OUT).
Clock input frequency	*10 MHz max*
High pulse width (clock input)	*15 ns min*
Low pulse width (clock input)	*25 ns min*
Gate width high	*25 ns min*
Gate width low	*25 ns min*
Input low voltage	*0.8 V max*
Input high voltage	*2.0 V min*
Output low voltage	*0.4 V max*
Output high voltage	*3.0 V min*

Configurable AUXIN<5:0>, AUXOUT<2:0> external trigger/clocks

The PCI-DAS6052 provides nine user-configurable trigger/clock pins available at the 100-pin I/O connector. Of these, six are configurable as inputs while three are configurable as outputs.

Table 20. Configurable triggers/clocks specifications

Parameter	Specification	
AUXIN<5:0> sources (SW selectable)	A/D CONVERT:	External ADC convert strobe
	A/D TIMEBASE IN:	External ADC pacer time base
	A/D START TRIGGER:	ADC Start Trigger
	A/D STOP TRIGGER:	ADC Stop Trigger
	A/D PACER GATE:	External ADC gate
	D/A START TRIGGER:	DAC trigger/gate
	D/A UPDATE:	DAC update strobe
	D/A TIMEBASE IN:	External DAC pacer time base
AUXOUT<2:0> sources (SW selectable)	STARTSCAN:	A pulse indicating start of conversion
	SSH:	Active signal that terminates at the start of the last conversion in a scan
	A/D STOP:	Indicates end of scan
	A/D CONVERT:	ADC convert pulse
	SCANCLK:	Delayed version of ADC convert
	CTR1 CLK:	CTR1 clock source
	D/A UPDATE:	D/A update pulse
	CTR2 CLK:	CTR2 clock source
	A/D START TRIGGER:	ADC Start Trigger Out
	A/D STOP TRIGGER:	ADC Stop Trigger Out
	A/D PACER GATE:	External ADC gate
	D/A START TRIGGER:	DAC Start Trigger Out
Default selections:	AUXIN0:	A/D CONVERT
	AUXIN1:	A/D START TRIGGER
	AUXIN2:	A/D STOP TRIGGER
	AUXIN3:	D/A UPDATE
	AUXIN4:	D/A START TRIGGER
	AUXIN5:	A/D PACER GATE
	AUXOUT0:	D/A UPDATE
	AUXOUT1:	A/D CONVERT
	AUXOUT2:	SCANCLK
Compatibility	5V/TTL	
Edge-sensitive polarity	Rising/falling, software selectable	
Level-sensitive polarity	Active high/active low, software selectable	
Minimum pulse width	3.75 nS	

DAQ-Sync inter-board triggers/clocks

The DAQ-Sync bus provides inter-board triggering and synchronization capability. Five trigger/strobe I/O pins and one clock I/O pin are provided on a 14-pin header. The DAQ-Sync signals use dedicated pins. Only the direction may be set.

Table 21. DAQ-Sync signal specifications

Connector	Signal names
DAQ-Sync	DS A/D START TRIGGER
	DS A/D STOP TRIGGER
	DS A/D CONVERT
	DS D/A UPDATE
	DS D/A START TRIGGER
	SYNC CLK

Power consumption

Table 22. Power consumption specifications

Parameter	Specification
+5 V	1.25 A typ, 1.5 A max. Does not include power consumed through the I/O connector.
+5 V available at I/O connector	1A max, protected with a resettable fuse

Environmental

Parameter	Specification
Operating temperature range	0 °C to 55 °C
Storage temperature range	–20 °C to 70 °C
Humidity	0% to 90% non-condensing

Mechanical

Table 23. Environmental specifications

Parameter	Specification
Card dimensions (L × W × H)	PCI half card: 174.4 (6.87) × 106.9 (4.21) × 11.65 mm (0.46 in.)

DAQ-Sync connector

Table 24. DAQ-Sync connector specifications

Parameter	Specification
Connector type	14-pin right-angle 100 mil box header
Compatible cables	MCC p/n: CDS-14-x, 14-pin ribbon cable. x = number of boards (2 to 5)

Table 25. DAQ-Sync connector pinout

Pin	Signal Name
1	DS A/D START TRIGGER
2	GND
3	DS A/D STOP TRIGGER
4	GND
5	DS A/D CONVERT
6	GND
7	DS D/A UPDATE
8	GND
9	DS D/A START TRIGGER
10	GND
11	RESERVED
12	GND
13	SYNC CLK
14	GND

SCSI connector

Table 26. SCSI connector specifications

Parameter	Specification
Connector type	Shielded SCSI 100 D-type
Compatible cables	C100HD50-x, unshielded ribbon cable. x = 3 or 6 feet
	C100MMS-x, shielded round cable. x = 1, 2, or 3 meters
Compatible accessory products (with the C100HD50-x cable)	ISO-RACK16/P ISO-DA02/P BNC-16SE BNC-16DI CIO-MINI50 CIO-TERM100 SCB-50
Compatible accessory products (with the C100MMS-x cable)	SCB-100

Table 27. 8-channel differential mode pinout

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	n/c
2	CH0 IN HI	52	n/c
3	CH0 IN LO	53	n/c
4	CH1 IN HI	54	n/c
5	CH1 IN LO	55	n/c
6	CH2 IN HI	56	n/c
7	CH2 IN LO	57	n/c
8	CH3 IN HI	58	n/c
9	CH3 IN LO	59	n/c
10	CH4 IN HI	60	n/c
11	CH4 IN LO	61	n/c
12	CH5 IN HI	62	n/c
13	CH5 IN LO	63	n/c
14	CH6 IN HI	64	n/c
15	CH6 IN LO	65	n/c
16	CH7 IN HI	66	n/c
17	CH7 IN LO	67	n/c
18	LLGND	68	n/c
19	n/c	69	n/c
20	n/c	70	n/c
21	n/c	71	n/c
22	n/c	72	n/c
23	n/c	73	n/c
24	n/c	74	n/c
25	n/c	75	n/c
26	n/c	76	n/c
27	n/c	77	n/c
28	n/c	78	n/c
29	n/c	79	n/c
30	n/c	80	n/c
31	n/c	81	n/c
32	n/c	82	n/c
33	n/c	83	n/c
34	n/c	84	n/c
35	AISENSE	85	DIO0
36	D/A OUT 0	86	DIO1
37	D/A GND	87	DIO2
38	D/A OUT1	88	DIO3
39	PC +5 V	89	DIO4
40	AUXOUT0 / D/A PACER OUT	90	DIO5
41	AUXOUT1 / A/D PACER OUT	91	DIO6
42	AUXOUT2 / SCANCLK	92	DIO7
43	AUXIN0 / A/D CONVERT / ATRIG	93	CTR1 CLK
44	D/A EXTREF	94	CTR1 GATE
45	AUXIN1 / A/D START TRIGGER	95	CTR1 OUT
46	AUXIN2 / A/D STOP TRIGGER	96	GND
47	AUXIN3 / D/A UPDATE	97	CTR2 CLK
48	AUXIN4 / D/A START TRIGGER	98	CTR2 GATE
49	AUXIN5 / A/D PACER GATE	99	CTR2 OUT
50	GND	100	GND

Table 28. 16-channel single-ended mode

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	n/c
2	CH0 IN	52	n/c
3	CH8 IN	53	n/c
4	CH1 IN	54	n/c
5	CH9 IN	55	n/c
6	CH2 IN	56	n/c
7	CH10 IN	57	n/c
8	CH3 IN	58	n/c
9	CH11 IN	59	n/c
10	CH4 IN	60	n/c
11	CH12 IN	61	n/c
12	CH5 IN	62	n/c
13	CH13 IN	63	n/c
14	CH6 IN	64	n/c
15	CH14 IN	65	n/c
16	CH7 IN	66	n/c
17	CH15 IN	67	n/c
18	LLGND	68	n/c
19	n/c	69	n/c
20	n/c	70	n/c
21	n/c	71	n/c
22	n/c	72	n/c
23	n/c	73	n/c
24	n/c	74	n/c
25	n/c	75	n/c
26	n/c	76	n/c
27	n/c	77	n/c
28	n/c	78	n/c
29	n/c	79	n/c
30	n/c	80	n/c
31	n/c	81	n/c
32	n/c	82	n/c
33	n/c	83	n/c
34	n/c	84	n/c
35	AISENSE	85	DIO0
36	D/A OUT 0	86	DIO1
37	D/A GND	87	DIO2
38	D/A OUT1	88	DIO3
39	PC +5 V	89	DIO4
40	AUXOUT0 / D/A PACER OUT	90	DIO5
41	AUXOUT1 / A/D PACER OUT	91	DIO6
42	AUXOUT2 / SCANCLK	92	DIO7
43	AUXIN0 / A/D CONVERT / ATRIG	93	CTR1 CLK
44	D/A EXTREF	94	CTR1 GATE
45	AUXIN1 / A/D START TRIGGER	95	CTR1 OUT
46	AUXIN2 / A/D STOP TRIGGER	96	GND
47	AUXIN3 / D/A UPDATE	97	CTR2 CLK
48	AUXIN4 / D/A START TRIGGER	98	CTR2 GATE
49	AUXIN5 / A/D PACER GATE	99	CTR2 OUT
50	GND	100	GND

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